MAY 6 1991

OTI-066 HIGH SPEED, 256 X 18 COLOR PALETTE VIDEO DAC

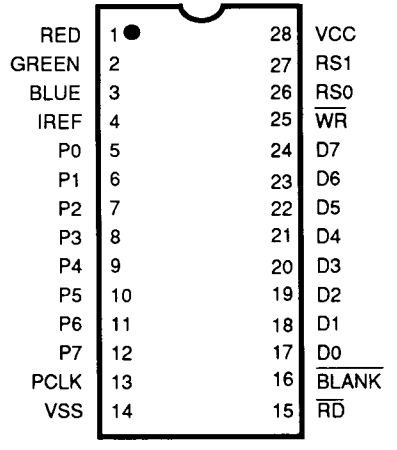
Description

The OTI-066 is a monolithic triple 6-bit video digital to analog converter (DAC) with 256 x 18 color palette for high-speed video applications. With this color palette, 256 color combinations out of 256K possible colors can be selected for display. A pixel mask is incorporated to allow for fast update of video information in a single cycle. The DAC on chip is capable of driving 75Ω or 37.5Ω standard loads at pixel rates of 65 MHz. All microprocessor interface I/O are TTL-compatible.

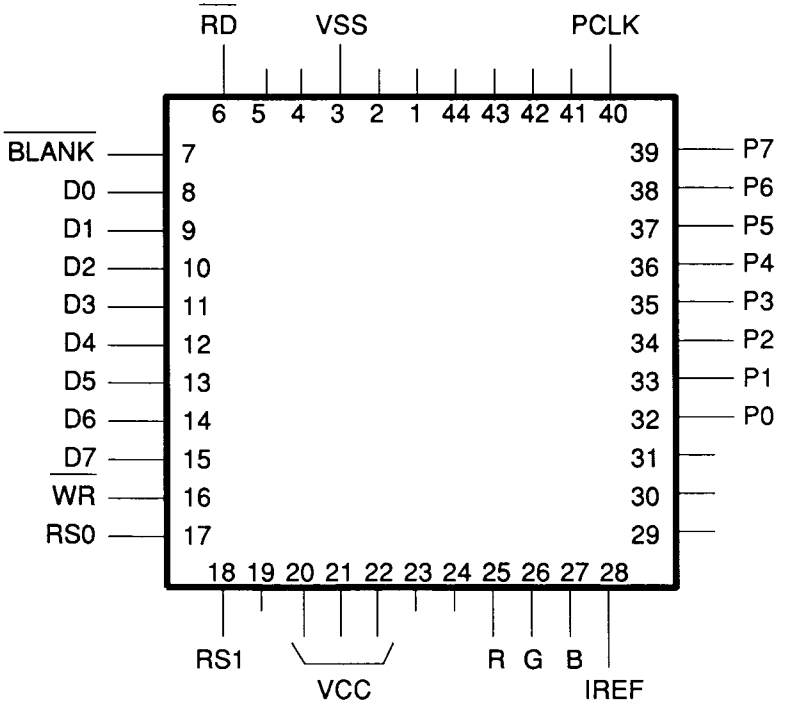
Features

- Pixel rate up to 65MHz
- 256 x 18 color palette
- Three internal 6-bit high speed DACs
- RGB analog outputs with composite blank
- Direct drive 75Ω or 37.5Ω load for video interface
- Microprocessor asynchronous interface
- TTL-compatible I/O interface
- Single +5-volt power supply
- Low power, high performance CMOS process
- Standard 600-mil, 28-pin DIP or 44-pin PLCC package
- RS170 video signal compatible
- Industrial standard part

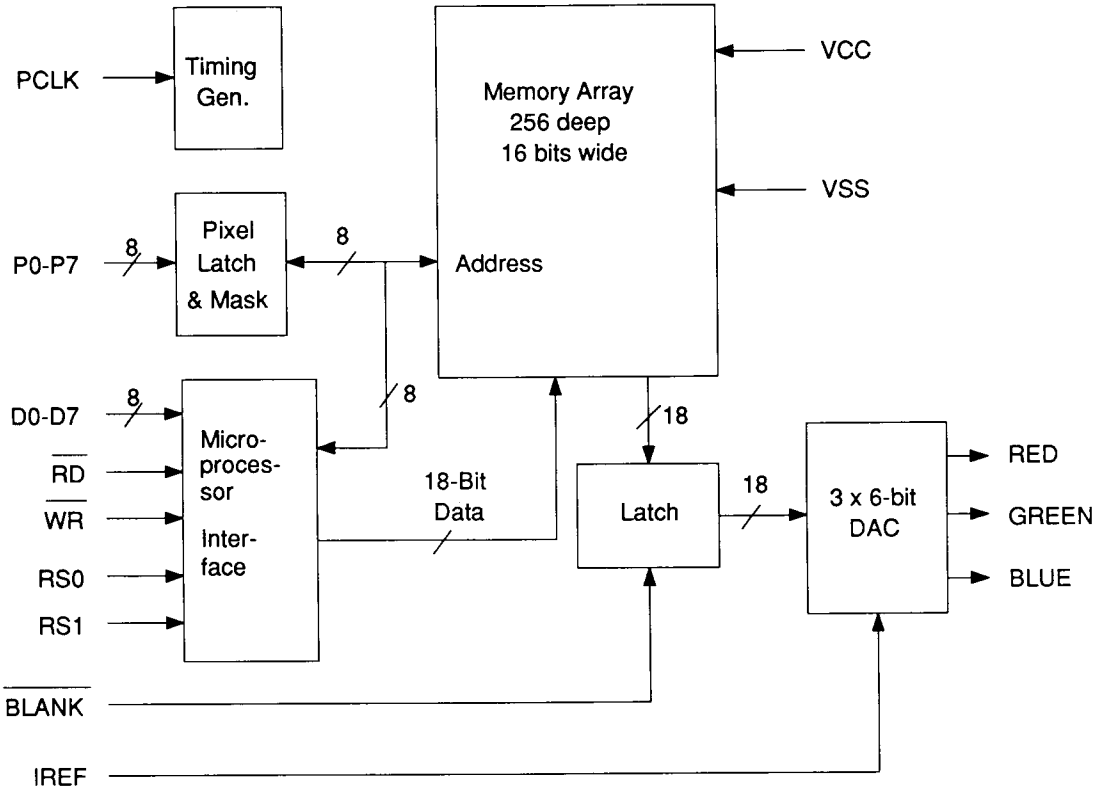
28-Pin Package



44-Pin Package



Circuit Block Diagram



Pin Descriptions

Signal Name	28-Pin DIP	44-Pin PLCC	Description
RED BLUE GREEN	1 2 3	25 26 27	These are the analog outputs of the 6-bit DACs. The RGB (red, blue, green) voltage will be developed at this output pin with the current flowing from this point into the terminating resistors. Each DAC is composed of 63 current sources. The output of these current sources is summed together based on the 6-bit binary value from the static RAM table.
IREF	4	28	The reference current forced out of this pin determines the current sourced by each of the 63 current sources in each of the 6-bit DACs. Each current source produces 1/30 of IREF when activated by the 6-bit digital code.
P0-P7	5-12	32-39	These are high-speed Pixel Address inputs. The address is latched and masked by the Pixel Register. It is used for addressing the Color Palette RAM and generating the final color value.
PCLK	13	40	This is the high-speed Pixel Clock signal. The rising edge samples and latches the Pixel Address and Blanking inputs. It controls progress of these values through the three-stage pipeline of the Color Palette and through the DACs to outputs.
VSS	14	3	Power supply ground.
$\overline{RD}$	15	6	Active low Read bus control signal. Enables Data I/O lines D0-D7. $\overline{RD}$ and $\overline{WR}$ should not be active at the same time.
$\overline{BLANK}$	16	7	Active low signal forces zero voltage at the DAC outputs. When $\overline{BLANK}$ is asserted, the Color Palette can still be updated through D0-D7.
D0-D7	17-24	8-15	Bi-directional data lines to read or write information for the OTI-066 internal registers. During the write cycle, the rising edge of $\overline{WR}$ latches the data into the selected register. The rising edge of $\overline{RD}$ determines the end of the read cycle. When $\overline{RD}$ and $\overline{WR}$ go high, the Data I/O lines will be in a tri-state mode.
$\overline{WR}$	25	16	Active low Write signal controls the timing of the write operations on the microprocessor interface inputs D0-D7. When asserted, the rising edge of $\overline{WR}$ will sample and latch data into internal registers. $\overline{RD}$ and $\overline{WR}$ signals should not be asserted at the same time.

Signal Name	28-Pin DIP	44-Pin PLCC	Description
RS0, RS1	26, 27	17, 18	Register Select inputs. These two inputs are sampled during the falling edges of the enable signals ($\overline{RD}$ or $\overline{WR}$) and select one of the three internal registers. Refer to "Internal Registers" for more information.
VCC	28	20-22	Positive power supply pin. It is normally connected to +5V and bypassed with a 10µF tantalum capacitor and a 0.1µF chip capacitor.

Internal Registers

There are three internal registers accessed using RS0 and RS1 that control addressing, color value, and pixel masking features.

RS1	RS0	Size (Bits)	Register Name	Description
0	0	8	Address (write mode)	Writing a value to this register performs the following operations. These operations precede writing one or more new color definitions to the color look-up table: a) Specifies an address within the color look-up table. b) Initializes the Color Value register.
1	1	8	Address (read mode)	Writing a value to this register performs the following operations. These operations precede reading one or more color definitions from the color look-up table: a) Specifies an address within the color look-up table. b) Loads the Color Value register with the contents of the location in the color look-up table addressed and then increments the Address register.
0	1	18	Color Value	The Color Value register is internally an 18-bit wide register used as a buffer between the microprocessor interface and the color look-up table. A value can be read from or written to this register by a sequence of three-byte transfers at this register address. When a byte is written, only the least significant six bits (D0-D5) are used. When a byte is read, only the

RS1	RS0	Size (Bits)	Register Name	Description
				least significant six bits contain information. The most significant two bits will be zero. The sequence of data transfer is RED, GREEN, then BLUE. After writing three values to this register, its contents are written to the location in the color look-up table specified by the Address register. The Address register then increments. After reading three values from this register, the contents of the location in the color look-up table specified by the Address register are copied into the Color Value register. The Address register then increments. Each transfer between the Color Value register and the color look-up table replaces the normal pixel mapping operation of the OTI-066 for a single pixel.
1	0	8	Pixel Mask	The Pixel Mask register can be used to mask selected bits of the Pixel Address value applied to the Pixel Address inputs (P0-P7). A '1' in a position in the mask register leaves the corresponding bit in the Pixel Address unaltered. A '0' sets the corresponding bit to zero. The Pixel Mask register does not affect the Address generated by the Microprocessor Interface when the look-up table is being accessed through that same interface.

Device Description

The OTI-066 is intended for use with the OTI-067 Extended High Resolution VGA controller. It contains a high-speed, random-access look-up table of 256 x 18-bit words, three 6-bit DACs, a microprocessor interface, and a pixel word mask. Figure 1 shows a block diagram of the OTI-066 in a low-cost VGA adapter, also using the OTI-067 VGA Graphics Controller and the OTI-069 Video Pixel Clock Generator.

An 8-bit value read on the Pixel Address inputs is used as a read address for the look-up table. This data is partitioned as three fields of 6 bits. Each field is applied to the inputs of a 6-bit DAC.

An externally generated blank signal can be input to the OTI-066. This signal acts on all three of the analog outputs. The BLANK signal is delayed internally so that it appears at the analog outputs with the correct relationship to the pixel stream.

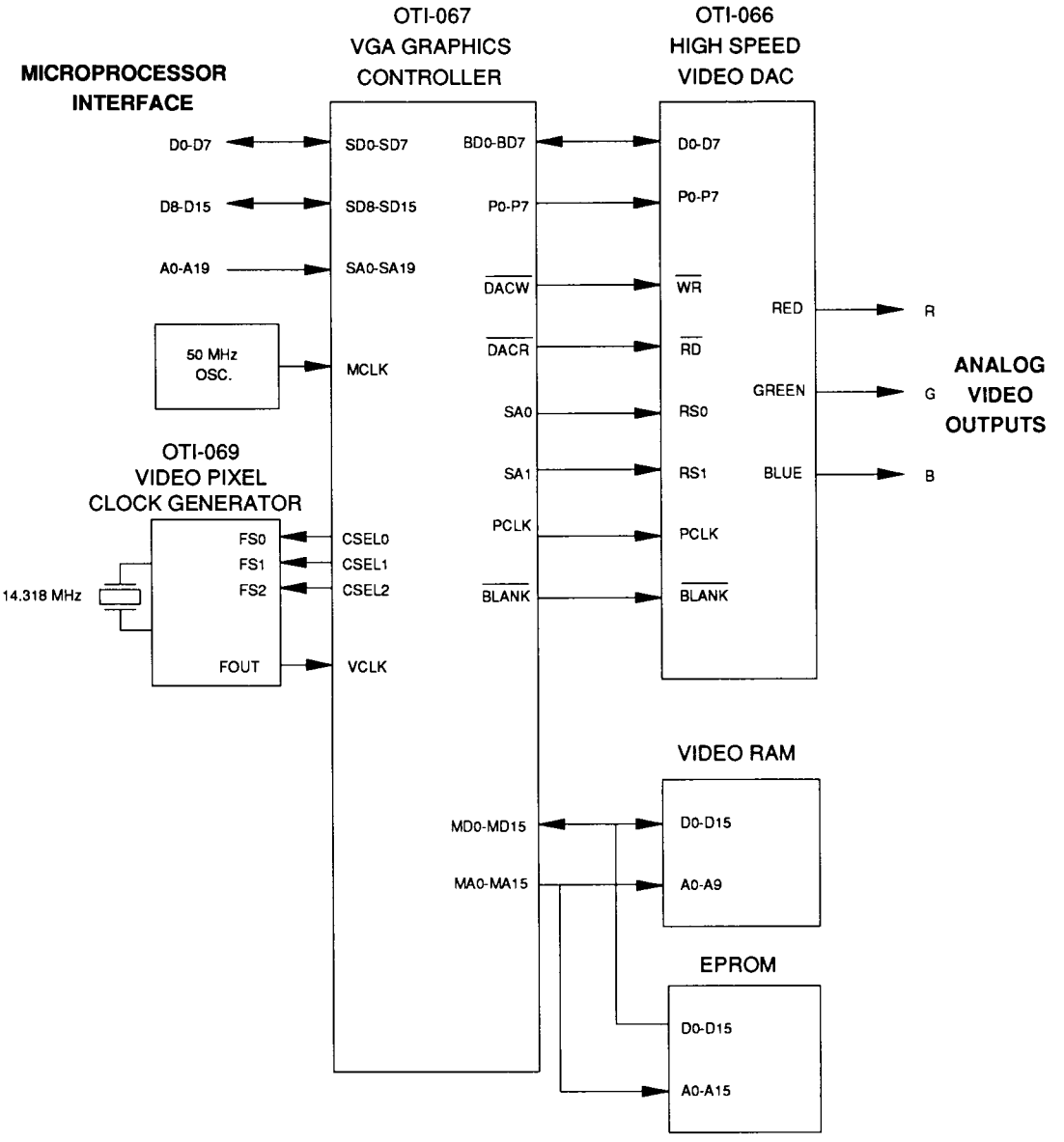


Figure 1. Typical Application

The contents of the look-up table are accessed via an 8-bit wide interface to the OTI-067. The use of an internal synchronizing circuit allows color value accesses to be totally asynchronous to the video path.

A pixel word mask is included to allow the incoming pixel address to be masked. This permits rapid changes to the effective contents of the color look-up table to facilitate such operations as animation and flashing objects. The pixel mask register is directly in the pixel stream, thus operations on the contents of the mask register should be synchronized to the pixel stream.

Video Path

Pixel address and $\overline{\text{BLANK}}$ inputs are sampled on the rising edge of the Pixel Clock. Their effect appears at the analog outputs after three further rising edges of the Pixel Clock (see Figure 2).

Analog Outputs

The outputs of the DACs are designed to be capable of producing 0.7-volt peak white amplitude with an IREF of 8.88 mA when driving a doubly terminated 75Ω load. This corresponds to an effective DAC output loading ($R_{effective}$) of 37.5Ω.

The $\overline{\text{BLANK}}$ input to the OTI-066 acts on all three of the analog outputs. When the $\overline{\text{BLANK}}$ input is low, a binary zero is applied to the inputs of the DACs.

The expression for calculating IREF with various peak white voltage/output loading combinations is:

$$IREF = \frac{V_{peak\ white}}{2.058 \times R_{effective}}$$

Note that for all values of IREF and output loading,

$$V_{BLACKLEVEL} = 0$$

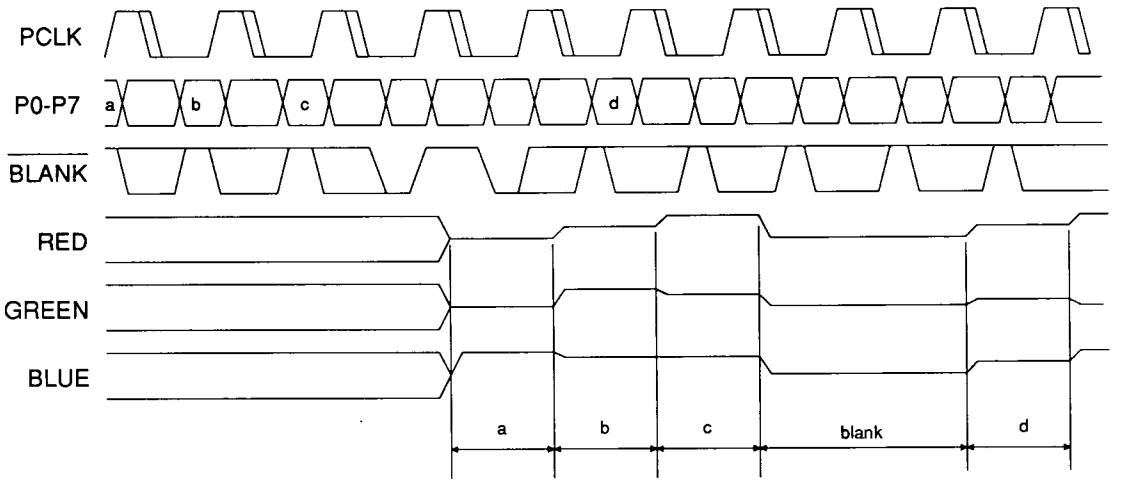


Figure 2

Microprocessor Interface

Below are listed the three microprocessor interface registers within the OTI-066 and the four locations through which they can be accessed:

RS1	RS0	Register Name
0	0	Address (write mode)
1	1	Address (read mode)
0	1	Color Value
1	0	Pixel Mask

The contents of the color look-up table can accessed via the Color Value register and the Address registers.

Writing to the look-up table – To set a new color definition, a value specifying a location in the color look-up table is first written to the write-mode Address register (RS0=0, RS1=0). The values for the red, green, and blue intensities are then written in succession to the color Value register. After *blue* data is written to the Color Value register, the new color definition is transferred to the color look-up table. The Address register is automatically incremented.

Since the Address register increments after each new color definition has been transferred from the color Value register to the color look-up table, it is simple to write a set of consecutive locations with new color definitions. First, the start address of the set of locations is written to the write mode Address register. Then, the color definitions for each location are written sequentially to the Color Value register.

Reading from the look-up table – To read a color definition, a value specifying the location in the look-up table to be read is written to the read-mode Address register. After this value has been written, the contents of the location specified are copied to the Color Value register. The Address register is automatically incremented.

The red, green, and blue intensity values can be read by a sequence of three reads from the Color Value register. After the *blue* value has been read, the location in the look-up table currently specified by the Address register is copied to the color Value register and then sequentially reading the color definitions for each location in the set.

Whenever the Address register is updated, any furnished color definition read or write is aborted and a new one may be begin.

Asynchronous look-up table access – Accesses to the Address and color Value registers can occur without reference to the high speed timing of the pixel stream being processed by the OTI-066. Internal logic synchronizes data transfers, between the look-up table and the color Value register, to the Pixel Clock in the period between the microprocessor interface accesses. Thus, various minimum periods are specified between microprocessor interface accesses to allow for the appropriate transfers to take place.

Pixel Mask register – The pixel address used to access the color look-up table through the pixel interface is the result of the bitwise ANDing of the incoming pixel address and the contents of the Pixel Mask register. This pixel masking process can be used to alter the displayed colors without altering the video memory or the look-up table contents. Thus, by partitioning the color definitions by one or more bits in the pixel address, such effects as rapid animation, overlays and flashing objects can be produced.

The Pixel Mask register is independent of the Address and Color Value registers. Operations on the Pixel Mask register are required to be synchronous to the pixel stream.

Electrical Specifications

Absolute Maximum Ratings*

Symbol	Parameter	Min.	Max.	Units
VCC	DC supply voltage	-0.3	7.0	volts
T_S	Storage temperature	-65	150	° C
T_A	Ambient temperature	-40	85	° C
PDmax	Power dissipation		1.0	W
	Reference current	-15		mA
	Analog output current (per output)		45	mA
	DC digital output current		25	mA

Notes:
*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes (1)
VCC	Positive supply voltage	4.5	5.0	5.5	volts	2
VSS	Ground		0		volts	
VIH	Input logic '1' voltage	2.0		VCC +0.5	volts	
VIL	Input logic '0' voltage	-0.5		0.8	volts	
T_A	Ambient operating temperature	0		70	° C	4
IREF	Reference current	-7.0		-10	mA	5

Notes:
1 All voltages are with respect to VSS unless otherwise specified.
2 This parameter allows for a range of fixed power supply voltages to be used. It does not imply that the supply voltage should be allowed to vary dynamically within these limits.
3 VIL(min) = 1.0V for a pulse width not exceeding 25% of the duty cycle (tCHCH) or 10 nS, whichever is the smaller value.
4 With a 400 linear ft/min transverse air flow.
5 Reference currents below the minimum specified may cause the analog outputs to become invalid.

DC Electrical Characteristics

Symbol	Parameter	Min.	Max.	Units	Notes (1,2,3)
ICC	Average power supply current		220	mA	4
VREF	Voltage at IREF input (pin 4)	VCC-3	VCC	volts	
IIN	Digital input current (any input)		±10	A	5,6
IOZ	Off state digital output current		±50	A	5,7
VOH	Output logic '1'	2.4		volts	IO = -5mA
VOL	Output logic '0'		0.4	volts	IO = 5mA

Notes:
1 All voltages are with respect to VSS unless otherwise specified.
2 The Pixel Clock frequency must be stable for a period of at least 20 µs after power-up (or after change in a Pixel Clock frequency) before proper device operation is guaranteed.
3 Over the range of the DC operating conditions unless specified otherwise.
4 IO = IO(max). ICC is dependent on digital loading and cycle rate, the specified values are obtained with the outputs unloaded and at the maximum rated Pixel Clock frequency.
5 VCC = max, VSS ≤ VIN ≤ VCC.
6 On digital inputs, pins 5-13, 15, 16, 25-27.
7 On digital input/output, pins 17-24.

DAC Characteristics

Symbol	Parameter	Min.	Max.	Units	Notes (1,2,3)
	Resolution	6		bits	
VO(max)	Output voltage		1.5	volts	IO 10 mA
IO(max)	Output current		-21	mA	VO 1V
	Full scale error		±5	%	4
	DAC to DAC correlation error		±2	%	5
	Integral linearity error		±0.5	LSB	6
	Rise time (10% to 90%)		8	nS	7
	Full scale setting time		20	nS	7,8,9
	Glitch energy		200	pVsec	7,9

Notes:

1 All voltages are with respect to VSS unless otherwise specified.
2 The Pixel Clock frequency must be stable for a period of at least 20 µs after power-up (or after change in a Pixel Clock frequency) before proper device operation is guaranteed.
3 Tested over the operating temperature range and at nominal supply voltage with IREF = -8.88 mA.
4 Full scale error from the value predicted by the design equations.
5 About the mid point of the distribution of the three DACs measured at full scale deflection.
6 Linearity measured from the best fit line through the DAC characteristic. Monotonicity guaranteed.
7 Load = 37.5Ω + 30 pF with IREF = -8.88 mA.
8 From a 2% change in the output voltage until setting to within 2% of the final value.
9 This parameter is sampled, not 100% tested.

AC Test Conditions

Input pulse levels	VSS to 3V
Typical input rise and fall times (10% to 90%)	3 nS
Digital input timing reference level	1.5V
Digital output timing reference level	0.8V and 2.4V
Digital output load	see Figure 3

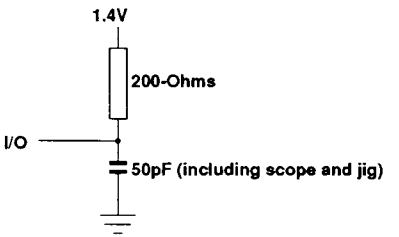


Figure 3.

Capacitance

Symbol	Parameter	Min.	Max.	Units	Notes (1,2)
CI	Digital input		7	pF	
CO	Digital output		7	pF	3
COA	Analog output		10	pF	4

Notes:

1 These parameters are sampled, not 100% tested.
2 Measured on a BOONTON METER.
3 $\overline{RD} \leq$ VIH(min) to disable D0-D7.
4 $\overline{BLANK} \leq$ VIL(max) to disable RED, GREEN, and BLUE.

Video Operation

Symbol	Parameter	Max.	Min.	Units	Notes (1,2)
tCHCH	PCLK period	10000	15.3	nS	
tCHCH	PCLK jitter	2.5		%	1
tCLCH	PCLK width low	10000	5	nS	
tCHCL	PCLK width high	10000	5	nS	
tPVCH	Pixel address set-up time		3	nS	2
tCHPX	Pixel address hold time		3	nS	2
tBVCH	BLANK set-up time		3	nS	
tCHBX	BLANK hold time		3	nS	
tCHAV	PCLK to valid DAC output	30	5	nS	3
tCHAV	Differential output delay	2		nS	4
	Pixel clock transition time	50		nS	

Notes:

1 This parameter allows for variation in the Pixel clock frequency, but does not permit the Pixel clock period to vary outside the minimum and maximum values for Pixel Clock (tCHCH) period specified above.
2 It is required that the Pixel Address input to the color look-up table be set up as a valid logic level with the appropriate set-up and hold times to each rising edge of PCLK (this requirement must be met during the blanking period).
3 A valid analog output is defined as when the changing analog signal is half-way between its successive values. This parameter is stable with time, but can vary between different devices and may vary with different DC operating conditions.
4 Between different analog outputs on the same device.

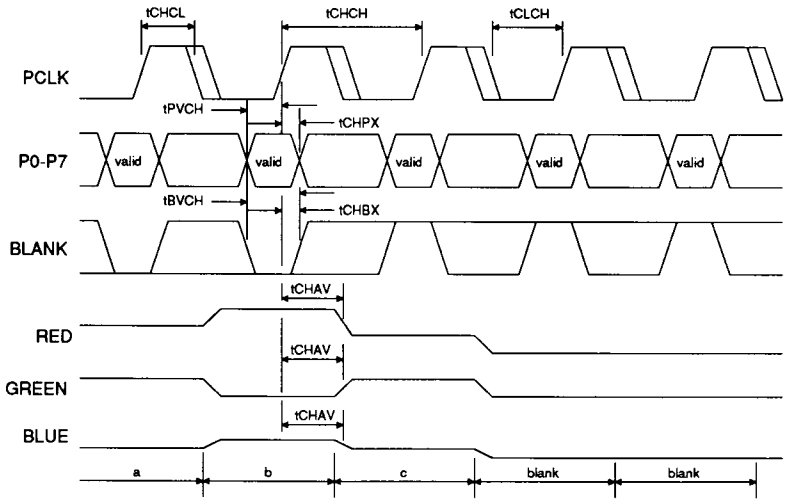


Figure 4.

Microprocessor Interface Timing Specifications

Symbol	Parameter	Max.	Min	Units	Notes
tWLWH	$\overline{WR}$ pulse width low		50	nS	
tRLRH	$\overline{RD}$ pulse width low		50	nS	
tSVWL	Register select set-up time		10	nS	
tSVRL	Register select set-up time		10	nS	
tWLSX	Register select hold time		10	nS	
tRLSX	Register select hold time		10	nS	
tDVWH	Write data set-up time	15	10	nS	
tWHDX	Write data hold time	15	10	nS	
tRLQX	Output turn-on delay	5	5	nS	
tRLQV	Read enable access time	40		nS	
tRHQX	Output hold time		5	nS	
tRHQZ	Output turn-off delay	20		nS	1
tWHWL1	Successive write interval		4τ	nS	3
tWHRL1	Write followed by read interval		4τ	nS	3
tRHRL1	Successive read interval		4τ	nS	3
tRHWL1	Read followed by write interval		4τ	nS	3
tWHWL2	Write after color write		4τ	nS	2, 3
tWHRL2	Read after color write		4τ	nS	2, 3
tRHRL2	Read after color read		7τ	nS	2, 3
tRHWL2	Write after color read		7τ	nS	2, 3
tWHRL3	Read after read address write		7τ	nS	2, 3
	Write/Read enable transition time	50		nS	

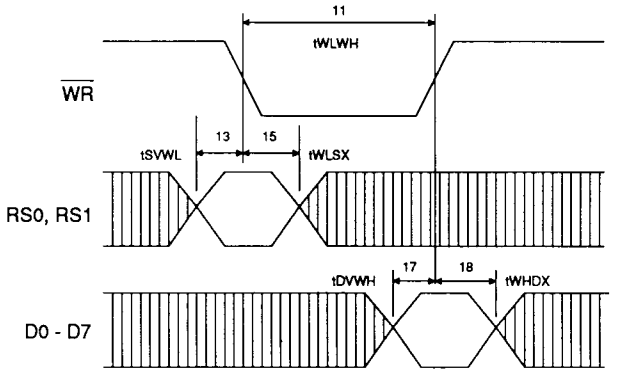
Notes:

1 Measure 200 mV from steady state output voltage

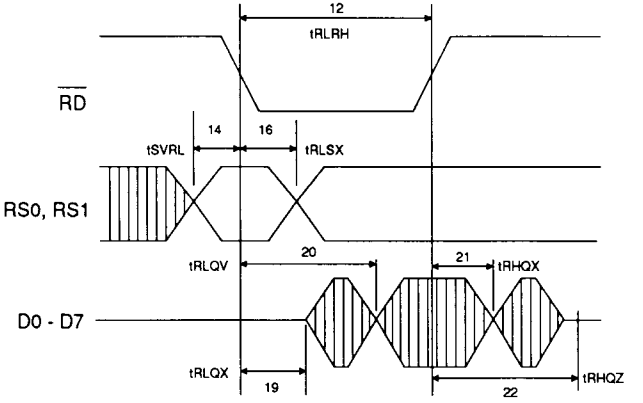
2 This parameter allows for synchronization between operations on the microprocessor interface and the pixel stream being processed by the color look-up table.

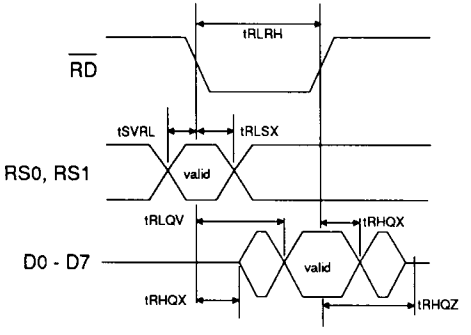
3 τ = PCLK period (tCHCH)

BASIC WRITE CYCLE

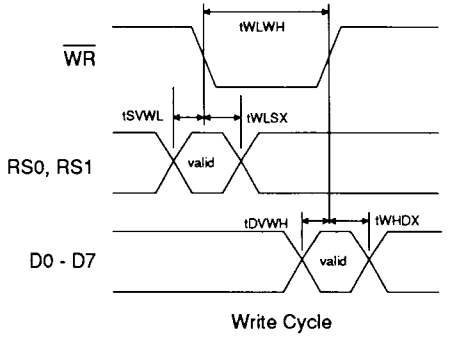


BASIC READ CYCLE





Read Cycle



Write Cycle

Figure 5.

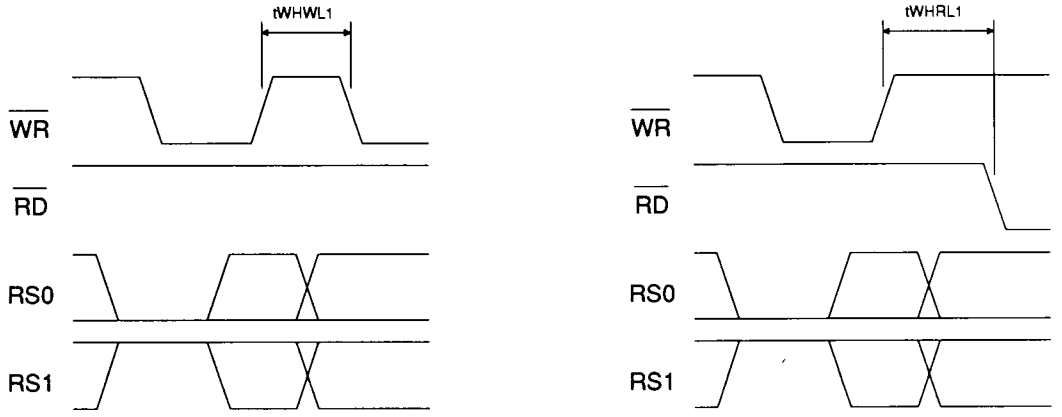


Figure 6.

Read from:
a) pixel mask register
b) pixel address register (read mode)
c) pedel address register (write mode)

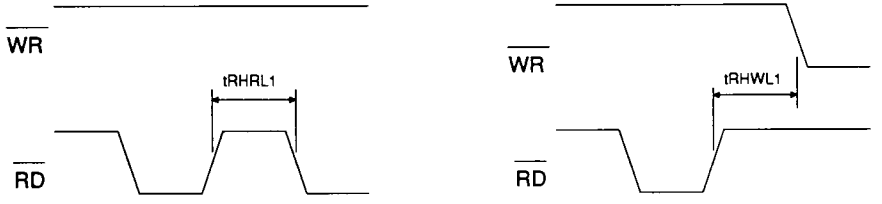
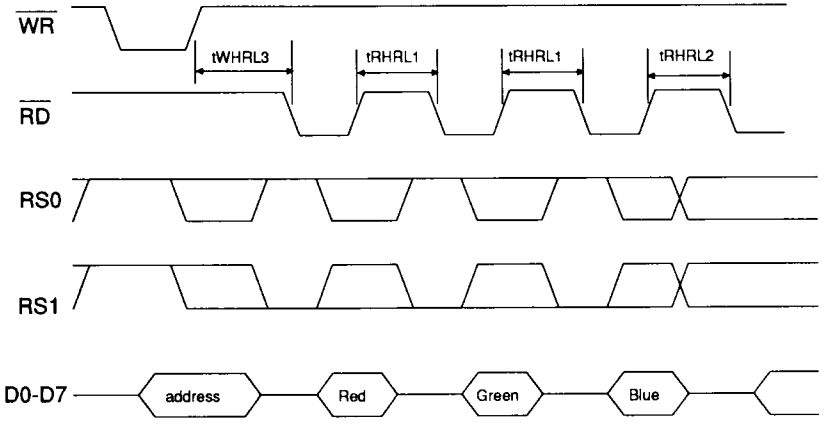


Figure 7.



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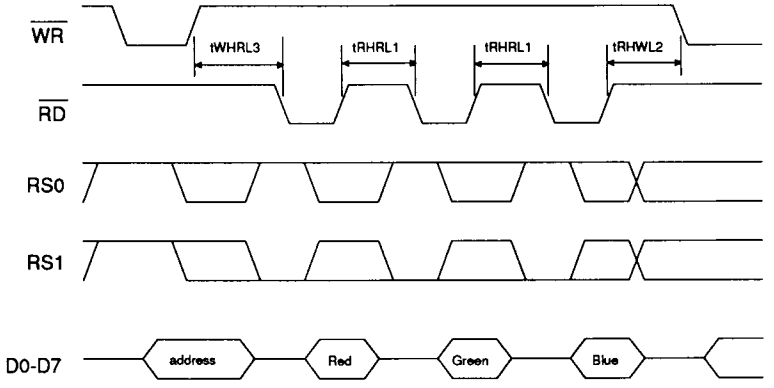


Figure 9.

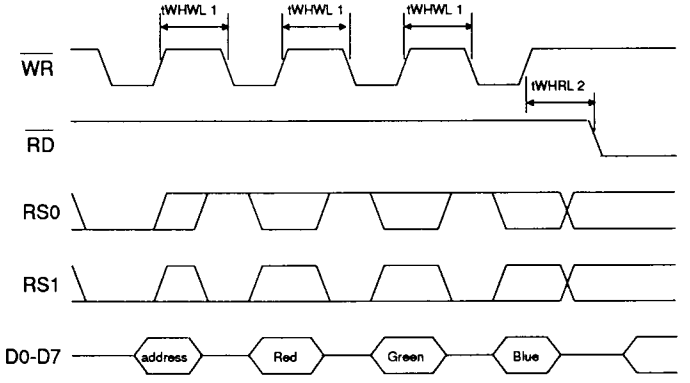


Figure 10.

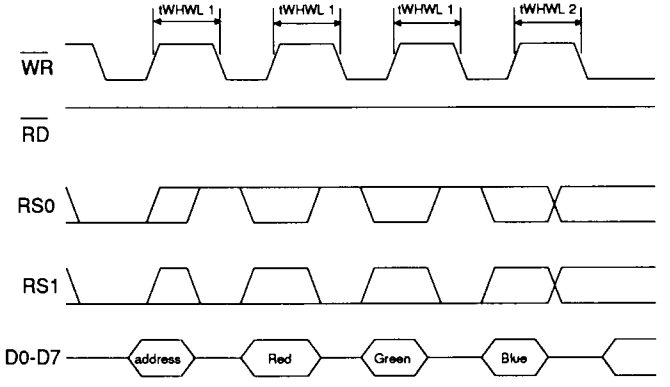
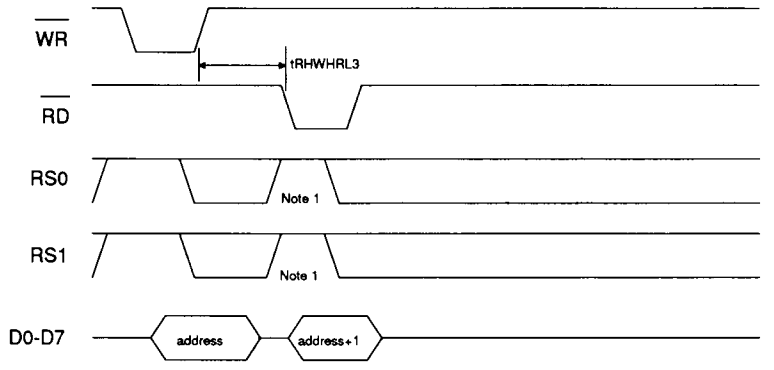
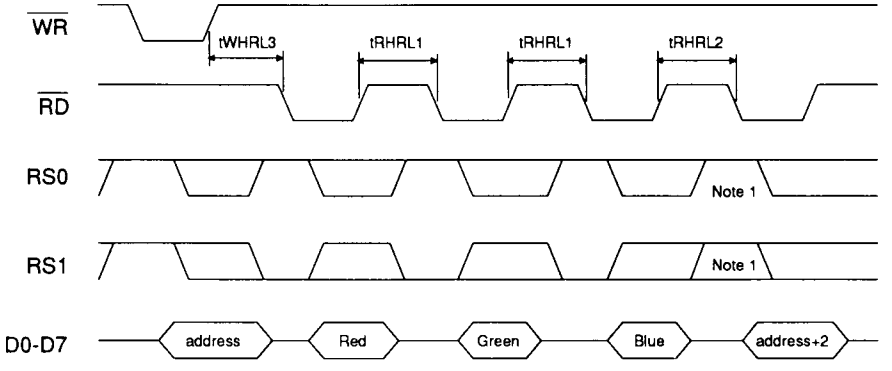


Figure 11.



Note 1: The timing for reading from address 0.0 is identical to that for reading from address 1.1.

Figure 12.



Note 1: The timing for reading from address 0.0 is identical to that for reading from address 1.1.

Figure 13.

Power Supply Decoupling

To supply the transient currents required by the OTI-066, the impedance in the decoupling path between VCC and VSS should be a 0.1μF high frequency capacitor in parallel with a larger tantalum capacitor with a value between 22μF and 47μF. An inductance may be added in series with the positive supply to form a low-pass filter and so further improve the power supply local to the OTI-066.

The combination of series impedance in the ground supply to the OTI-066 and transients in the current drawn by the OTI-066 will appear as differences in the VSS voltages to the OTI-066 and to the digital devices driving it. To minimize this differential ground noise, the impedance in the ground supply between the OTI-066 and the digital devices driving it should be minimized.

Analog Output Line Driving

The DACs in the OTI-066 are made from summed, switched current sources. IREF sets the current sourced by each current source, the digital input to each DAC determines how many current sources are active. The load resistance between the DAC output and VSS determines the voltage produced by each DAC.

The connection between the DAC outputs of the OTI-066 and the RGB inputs of the monitor it is driving should be regarded as a transmission line. Impedance changes along the transmission line will result in the reflection of part of the video signal back along the transmission line. These reflections may result in a degradation of the picture displayed by the monitor. To insure good signal fidelity, RF techniques should be observed. The PCB trace connecting the OTI-066 to the offboard connector should be sized so as to form a transmission line of the correct impedance. Correctly matched RF connectors should be used to connect from the PCB to the coaxial cable, and from the cable to the monitor being driven.

Two methods of DAC termination and their relative merits are described here.

Double termination – A load resistor is placed at both the DAC output and the monitor input. The resistor values should be equal to the characteristic impedance of the line.

Double termination of the DAC output allows both ends of the transmission line between the DAC outputs and the monitor inputs to be correctly matched, and, thus, should result in an ideal reflection-free system.

This arrangement is relatively tolerant to variations in transmission line impedance (e.g., a mismatched connector) since no reflections occur from either end of the line.

Also, the rise time of the DAC outputs is dependent on the RC time constant of the load it is driving. Thus, a double-terminated DAC output will rise faster than any singly terminated output.

Analog Output – Protection

CMOS devices are susceptible to damage from high electrostatic voltages. Normal antistatic precautions should be observed when handling the OTI-066 during system manufacture.

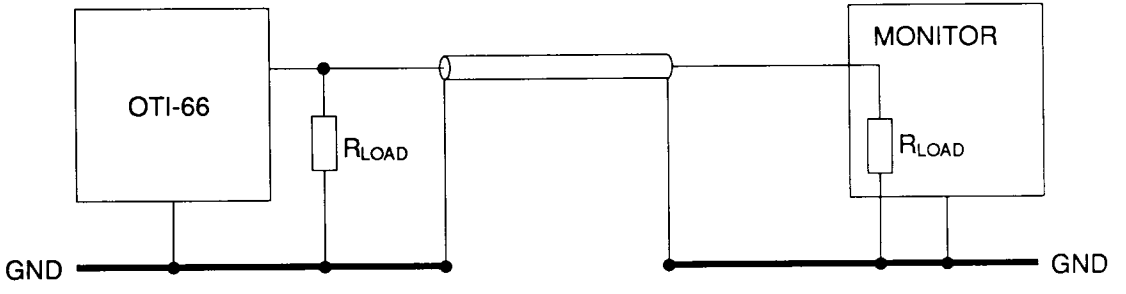


Figure 14.

Once assembled into a system, devices are much less exposed to static damage. However, if the analog outputs of the OTI-066 are made available at connectors outside the graphic system, they are still exposed to static damage and other hazardous voltages. Protection devices (e.g., IN4148 or any low cost silicon diode) should be considered at this exposed interface (see Figure 15).

Digital Input Termination

The PCB trace lines between the outputs of the TTL devices driving the OTI-066 behave like low impedance transmission lines driven from a low impedance source terminated with a high impedance. In accordance with transmission line principles, signal transitions will be reflected from the high impedance input to the OTI-066. Similarly, signal transitions will be inverted and reflected from the low impedance TTL output. To reduce or eliminate the ringing and in particular the undershoot that reflections cause, line termination is recommended. The termination may either be series or parallel.

The recommended technique is to use series termination. Series termination has the advantage of drawing no DC current and using fewer components. Series termination is accomplished by placing a resistor in series with the signal line at the outut of the TTL driver. This matches the TTL output impedance to that of the transmission line and so ensures that any signal incident on the TTL output is not reflected.

Current Reference – Design

To ensure that the output current of the DACs is predictable and stable with temperature variations, an active current reference is recommended. Figure 16 shows four designs of current reference.

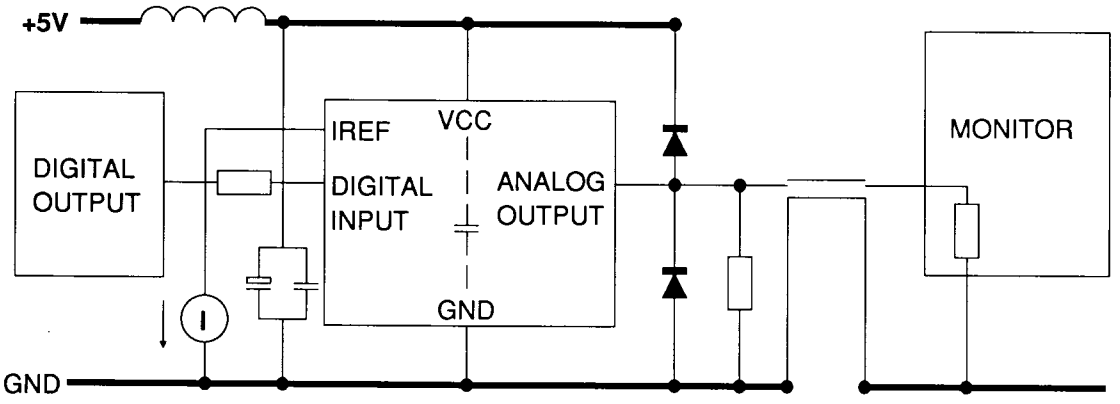


Figure 15.

Figure 16d shows the use of the LM334 precision current source as a current reference. It is shown in its temperature compensated configuration. The reference current is set by a single resistor (15Ω in this case) and is independent of the value of VCC.

Figures 16a-c are similar circuits. Each circuit uses three resistors and the power supply voltage to set the reference current IREF through a transistor. In circuit 16b and 16c, the thermal variations in the base-emitter voltage of the transistor are compensated by the use of a forward-biased diode (a transistor acting as a diode in the case of circuit 16c).

Current Reference – Decoupling

The DACs in the OTI-066 are made from switched current sources which are based around a current mirror. The total current output by each DAC is determined by the number of active current sources and the reference current IREF.

As long as any supply variations are minor, or a suitably high quality current reference is used which tracks the variations, then no coupling capacitors need to be used.

However, voltage variations on the supply not managed by the current reference circuit will result in variations in the DAC output current. If the bandwidth of the current reference circuit is not sufficient to

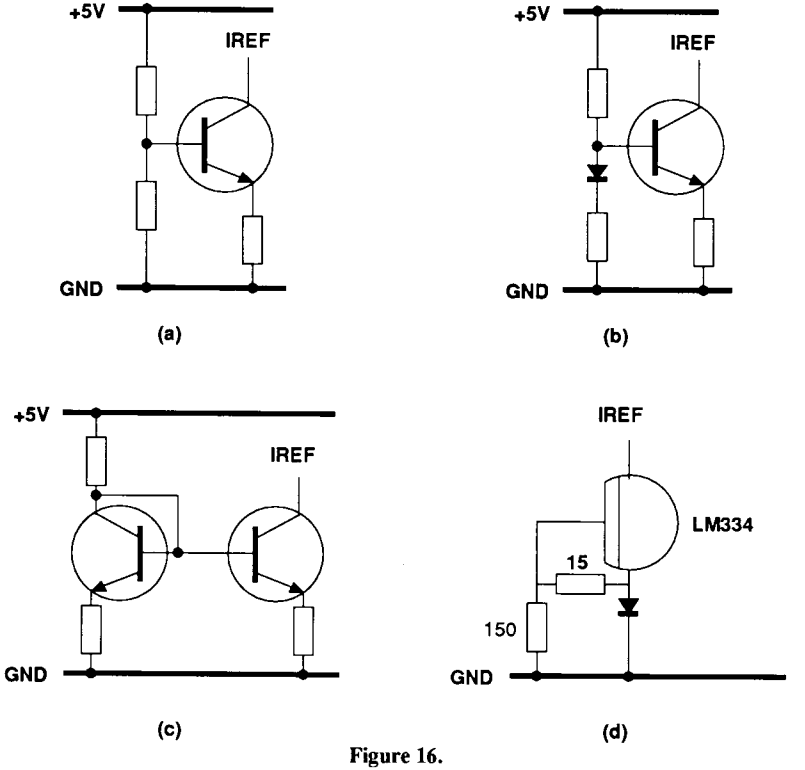


Figure 16.

track these supply variations, it is recommended that a coupling capacitor (47μF to 100μF) in parallel with a high frequency capacitor of 100 nF should be used to couple the IREF input to VCC. This will enable the current reference to track both low and high frequency variations in the supply.